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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,379	11/20/2003	Hiroshi Uragami	4597	2559

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,379	URAGAMI ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 5-8 is withdrawn in view of the newly discovered reference(s) to Takado (JP/05198707). Rejections based on the newly cited reference(s) follow.

Claim Objections

2. Claims 5, 6, 7, 10, 11 and 12 are objected to because of the following informalities:

Claim 5 recites "said resin material" in lines 7, 8 and 14. The examiner respectfully suggests changing "said resin material" to --said **solid** resin material-- in order to maintain proper antecedent basis and consistency through the claim language. Appropriate correction is required.

Claim 6 recites "said resin material" in lines 3 and 5. The examiner respectfully suggests changing "said resin material" to --said **solid** resin material-- in order to maintain proper antecedent basis and consistency through the claim language. Appropriate correction is required.

Claim 7 recites "said resin material" in lines 7, 4, 5 and 7. The examiner respectfully suggests changing "said resin material" to --said **solid** resin material-- in order to maintain proper antecedent basis and consistency through the claim language. Appropriate correction is required.

Claim 10 recites "The resin material" in line 1. The examiner respectfully suggests changing "The resin material" to --The **solid** resin material-- in order to maintain proper antecedent basis and consistency through the claim language. Appropriate correction is required.

Claim 10 recites "said resin material" in lines 3, 5 and 6. The examiner respectfully suggests changing "said resin material" to --said **solid** resin material-- in order to maintain proper

antecedent basis and consistency through the claim language. Appropriate correction is required.

Claim 11 recites "The resin material" in line 1. The examiner respectfully suggests changing "The resin material" to --The **solid** resin material-- in order to maintain proper antecedent basis and consistency through the claim language. Appropriate correction is required.

Claim 11 recites "said resin material" in line 2. The examiner respectfully suggests changing "said resin material" to --said **solid** resin material-- in order to maintain proper antecedent basis and consistency through the claim language. Appropriate correction is required.

Claim 12 recites "The resin material" in line 1. The examiner respectfully suggests changing "The resin material" to --The **solid** resin material-- in order to maintain proper antecedent basis and consistency through the claim language. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 5- 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Takado (JP/05198707).

Re claims 5 and 8, Takado discloses a method of resin-encapsulating an electronic component (i.e., method of manufacturing resin-encapsulated a semiconductor device) on a main surface of a board, using a mold pair having an upper mold (7) and a lower mold (1) and a solid

resin material (2A) for resin encapsulation (10), comprising the steps of placing the board on the lower mold (1) (see Drawings 1-4); placing the resin material (2A) on a main surface of the board (see Drawing 4) such that the resin material (2A) is not in contact with a conductive material (i.e., the metal line 5) connecting an electrode of the board with an electrode of the electronic component (see Drawing 4); closing the mold pair (see Drawing 4 and 5); generating melted resin (1B) on the main surface of the board (see Drawing 5) and enclosing the electronic component in the melted resin by heating the resin material (see Drawings 4 and 5); and forming a resin mold product by setting said melted resin (see Drawings 1-7 and related text in Abstract and Detailed Description of the Invention).

Re claim 6, as applied to claim 5 above, Takado discloses all the claimed limitations including the limitation wherein the resin material has such size and shape that correspond to size and shape of the cavity; and the melted resin is generated by heat transmitted from the upper mold to the resin material (see Drawings 1-7 and related text in Abstract and Detailed Description of the Invention).

Re claim 7, as applied to claim 5 above, Takado discloses all the claimed limitations including the limitation wherein the resin material is formed such that a space formed by the board and the resin material encloses the electronic component, when the resin material is placed on the main surface of the board; and the space is set to have such a size that the resin material is not in contact with the conductive material connecting the electrode of the board with the electrode of the electronic component (see Drawings 1-7 and related text in Abstract and Detailed Description of the Invention).

Re claim 9, Takado discloses a solid resin material consisting of a solid resin material adapted, sized and shaped to placed in a mold cavity provided in a mold pair, and adapted to be used as a raw material for being melted in the cavity to produce thereof a melted resin in a

method of resin-encapsulating an electronic component mounted on a main surface of a board in thecavity by encapsulating the electronic component in the melted resin and setting the melted resin in the cavity, wherein the solid resin material has such a size and a shape that correspond to a size and a shape of the cavity (see Drawings 1-7 and related text in Abstract and Detailed Description of the Invention).

Re claim 10, as applied to claim 9 above, Takado discloses all the claimed limitations including the limitation the resin formed adapted, sized and such that a space formed by the board and the resin material encloses the electronic component, when the resin material is placed on the main surface of the board; wherein the space is set to have such a size that the resin material is not in contact with a conductive material connecting an electrode of the board with an electrode of said electronic component (see Drawings 1-7 and related text in Abstract and Detailed Description of the Invention).

Re claim 11, as applied to claim 9 above, Takado discloses all the claimed limitations including the limitation wherein a notch is formed in said resin material (see Drawings 1-7 and related text in Abstract and Detailed Description of the Invention).

Re claim 12, as applied to claim 9 above, Takado discloses all the claimed limitations including the limitation the resin material being a solid plate consisting of the solid resin material and having a stepped sectional shape with stepped side walls (see Drawings 1-7 and related text in Abstract and Detailed Description of the Invention).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takado (JP/05198707) in view of Utsumi et al. (US/6,081,978).

Re claims 1 and 4, Takado discloses a method of resin-encapsulating an electronic component (i.e., method of manufacturing resin-encapsulated a semiconductor device) mounted on a main surface of a board, using a mold pair having an upper mold and a lower mold, comprising the steps of: attaching the board on one of the upper or lower mold (see Drawings 3 and 4); generating melted resin (10) in a cavity provided in lower mold (1) (see Drawings 1 and 2) by melting a solid resin material (2A) (see Drawings 1 and 2) in the cavity (see Drawings 4-6); immersing said electronic component in the melted resin in said cavity by closing said mold pair (see Drawings 4-6); and forming a resin molded product including said electronic component in a set resin by setting the melted resin to produce the set resin in the cavity (see Drawings 1-7 and related text in Abstract and Detailed Description of the Invention).

However, Takado does not specifically disclose attaching of the board on the upper mold.

Utsumi et al. disclose a method of resin-encapsulating electronic component (i.e., semiconductor device) the method includes attaching the board on the upper mold (31a) (see Fig. 1(a)) and contacting the upper mold (31a) and lower mold (31b) in order to form resin-encapsulated electronic device (i.e., resin encapsulated semiconductor device).

Both Takado and Utsumi et al. teachings are directed to fabrication process of encapsulating an electronic device (i.e., semiconductor device) using thermosetting resin. Therefore, the teachings of Takado and Utsumi et al. are analogous.

Hence, one of ordinary skill in the art would have been motivated to look to analogous art teaching of attaching of the board on the upper mold and contacting the upper mold (31a) and

lower mold (31b) in order to form resin-encapsulated electronic device as discloses by Utsumi et al.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Takado reference with attaching of the board on the upper mold as taught by Utsumi et al. in order to form resin-encapsulated electronic device (i.e., resin encapsulated semiconductor device) by closing the mold pair.

Re claim 2, as applied to claim 1 above, Takado and Utsumi et al. in combination disclose all the claimed limitations including placing the solid resin material placed in the cavity prior generating melted resin (see Takado Drawings 1-7 and related text in Abstract and Detailed Description of the Invention and Utsumi et al. Figs. 1(a)-1(c)).

Re claim 3, as applied to claim 1 above, Takado and Utsumi et al. in combination disclose all the claimed limitations including the limitation wherein an electrode of the board and an electrode of said electronic component are connected by a conductive material forming a loop in a prescribed plane; and in the step of immersing said electronic component in the melted resin, said prescribed plane moves substantially vertically to a main surface of the melted resin (see Takado Drawings 1-7 and related text in Abstract and Detailed Description of the Invention and Utsumi et al. Figs. 1(a)-1(c)).

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takado (JP/05198707) in view of Utsumi et al. (US/6,081,978), as applied in Paragraph 6 above, and further in view of Kawai et al. (JP/01097622).

Re claim 13, as applied to claim 1 in Paragraph 6 above, Takado and Utsumi et al. in combination disclose all the claimed limitations including transporting means of the solid resin into the cavity.

However, the combination of Takado and Utsumi et al. do not specifically disclose using a vacuum-holding conveyor during placing of the solid resin material in the cavity.

Kawai et al. disclose use of molding apparatus that equipped with a vacuum conveyor to transport the resin sheet back and forth during the molding process (see Abstract).

Takado, Utsumi et al. and teachings Kawai et al. are directed to fabrication process of encapsulating an electronic device (i.e., semiconductor device) using thermosetting resin. Therefore, the teachings of Takado, Utsumi et al. and teachings Kawai et al. are analogous.

Hence, one of ordinary skill in the art would have been motivated to look to analogous art teaching of use of molding apparatus that equipped with a vacuum conveyor to transport the resin sheet back and forth during the molding process as discloses by Kawai et al.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Takado and Utsumi et al. reference with use of molding apparatus that equipped with a vacuum conveyor as taught by Kawai et al. in order to transport the resin sheet back and forth during the molding process.

Response to Arguments

8. Applicants' arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. **THIS ACTION IS MADE NON-FINAL.**

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Inoue et al. (US/5,733,802) also disclose similar inventive subject matter.

Correspondence

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

BK
April 26, 2005